ABSTRACT OF THE DISCLOSURE

A slow decode control part divides a reference clock generated by a VCXO at a ratio of a slow speed to a normal speed. An STC circuit counts the divided clock. A time for starting decoding by an MPEG video decode part is decided by comparing a DTS included in MPEG data with the count of the STC circuit. A display time determination part determines a timing for outputting decoded data by comparing a PTS included in the MPEG data with the count of the STC circuit. Decoded data temporarily held in a frame buffer is output in response to a signal generated in a determination part on the basis of frame frequency information included in the MPEG data. Thus, slow reproduction is implemented with a high degree of freedom not limited to an integer-fractional speed without requiring a complicated circuit structure.